

S/N 10/057,225

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner: Michael Trinh

Serial No.: 10/057,225

Group Art Unit: 2822

Filed: January 25, 2002

Docket: 303.506US4

Title: METHOD OF FABRICATING A TRANSISTOR ON A SUBSTRATE TO OPERATE  
AS A FULLY DEPLETED STRUCTURE



COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/145100 6104068	September 1, 1998	303.506US1	STRUCTURE AND METHOD FOR IMPROVED SIGNAL PROCESSING
09/560777 6413825	April 28, 2000	303.506US2	METHOD FOR SIGNAL PROCESSING
09/560917 6355961	April 28, 2000	303.506US3	STRUCTURE AND METHOD FOR IMPROVED SIGNAL PROCESSING
09/144202 6320222	September 1, 1998	303.517US1	STRUCTURE AND METHOD FOR REDUCING THRESHOLD VOLTAGE VARIATIONS DUE TO DOPANT FLUCTUATIONS

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

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Date

29 June 2004

By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29th day of June, 2004.

Name

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Signature

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